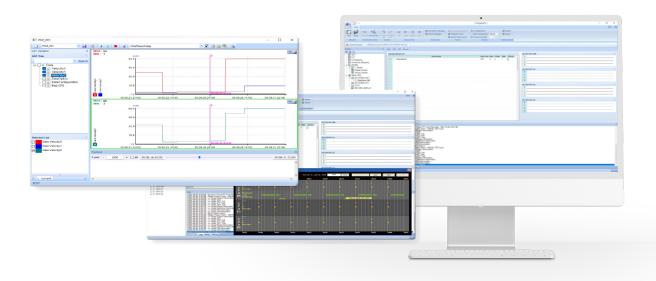


RTNgine Software

RTNgine Software

RTNgine software a real-time simulation engine for Avionics SIL and FLCC HILS configurations, is a key program to control, simulate and manage all equipment interlinked with the operation a nd testing of the equipment.



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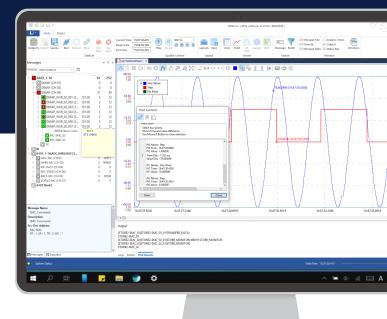
RTNgine a key software to establish simulation and integrated testing environment based on real-time, provides convenient development environment and allows user to form testing equipment easily, quickly and efficiently.

- Based on various testing tools, it is a main program that is optimized for simulation performance /test, analysis, error and detection.
- Possible to input a lot of data and error and analyze them accurately and variously.
- Supports recent Matlab/Simulink and execute ICD, Behavior and Dynamic model on real-time.
- Provides I/O control technology that expand CPU and I/O interface easily.



Highlights

- Control and execute model precisely by Sub Frame basis
- Support for Frame Scheduler to ensure execution priority between models
- Execution synchronization technology among multiple CPU
- GST data synchronization technology among multiple CPU
 - Share data by variable type and bit basis
 - Share Union data
- Provides I/O control technology that expand CPU and I/O interface easily
- IO Mapping Middleware which connects simulation variable and IO Input-Output
- Measure execution procedure and time of all scheduled IO and model
- Process Injection real-time data
- Transfer real-time data using network or shared memory



System Architecture

| RTNgine STE | Configuration | GST Editor | IO Mapping | Universal Mapping | SIM Manager | Sched Monitor |
|---|--|------------|--------------------------|------------------------|------------------|------------------|
| | Model Manager | Data view | Dynamic TST Injection | Strip Chart Plotter | Record Replay | ВІТ |
| RTNgine Core Simulation Control / Real-time Processing / Model Scheduling (HILS Model, 6D0F Model) | | | | | | |
| RTNgine Drv | Real-time IO Device Driver (MIL-STD-1553B, ARINC429, CAN, SDLC, Serial, Ethernet, AIO, DIO, RFM, ScramNet···etc) | | | | | |
| RTNgine Bench | RTOS(VxWorks) (Real-time Processor, IO Module, SCU, IOB, FIU, TP&BOB, IFB···etc) | | | | | |



RTNgine STE

RTNgine STE is integrated development environment which is able to develop simulation Logic based on project and execute verification for operation.

Main Function

• Model Manager: Logic Model, Matlab import

■ GST Editor: variable create, GST/IOT from ICD

■ Configuration : Hardware Control

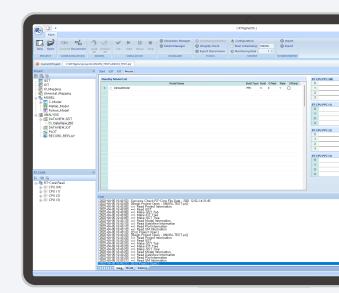
■ Data View : Monitoring, Value Set

Strip Chart : 2D Data Monitoring

■ Record & Replay : Data recording & playback

• Simulation Manager : Simulation condition setup

■ IO Mapping: Configuration setup for Interface data between IO and GST



Details Function

| GTS / IOT | Testing environment of RTNgine is executed basically based on GST (Global Simulation Table). GST is a breakup real-time database possessing all dynamic data of RTNgine as global variables defined by user for each project. GST manufactures using GST Editor and Import provided from RTNgine. IOT is a table generated by input/output devices and defines the actual output IO values. | | |
|---------------------|---|---|--|
| | Provide GST/IOT EditorInterface IO MappingModel Variable MappingBit Variable | Union Keyword Integration for ICD Management Tool or System Bridge Tool | |
| GTS / IOT Editor | Declare GST VariableBit VariableUse Union KeywordReady defined variable type | Loading ready defined Header fileError CheckSave & Build GST File | |



Details Function

| Simple IO Mapping | Connect input-output data (such as digital signal and analog signal, etc.) to GST variable and control IO Possible to execute Mapping between Model variable and GST with just user's double click. Auto Mapping function that applied by name and rule | | | | |
|-------------------------|---|--|--|--|--|
| | · Provides function for setting message of various I/O interface and mapping GST | | | | |
| Universal Mapping | · M1553 - Set BC, RT, BM message - BC, RT, BM message GST Mapping | SerialSet TX, RX messageCombine message packetMessage Mapping | | | |
| | · A429 - Set message - Message GST Mapping | · CAN - Set TX,RX message - Message Mapping | | | |
| | Form model directly and import 3 rd party Model (Matlab, C, C++, Fortran) | | | | |
| Model Manager | Form C Model directly or load Model already written before Load model formed with Matlab through Model Manager | Load by selecting variables by type used at Matlab.Check and control Matlab variables through GST and Mapping | | | |
| | Support Hard Real-Time based on VxWorks and measure execution time through Scheduling Monitor | | | | |
| Realtime Performance | Measure execution time of model data by Micro sec Provides a scheduling monitor to check the scheduling status | Check time of I/O ProcessCheck time among various ModelRecord function output to Excel Format | | | |
| | Run the built model by allotting it to Real-Time Core based on this GST | | | | |
| Execution | Support Multi CPU Possible to use main scheduling separately according to working method | Allot easy model with Drag & Drop waySupport Hard Real-Time | | | |
| | Select GST required monitoring and monitor this data through Data View | | | | |
| Monitoring Data | Select GST at left side Tree Allows user to set the desired value in the Value line Display timeline currently being simulated | · Display Hex, Bin and Plot type | | | |
| | Select GST required monitoring and provide plot function of this data | | | | |
| Monitoring Plot | Select right side ChartSelect GST at left side Tree | Select GST repeatably after adding ChartAvailabe to move desired time zone at Control | | | |



Details Function

Data Injection Tool

Possible to inject data and error to input-output data while testing and simulation are executed.

- · Monitor and save variable value
- · Input data and noise signal
- Constant, Sine, Triangle, Ramp, Step, Pulse, Random
- · Possible to convert data unit and display them
- · Manage setting list of data input

★ Update: RTNgine ver.3.6

| Multi-Core | T2080 based Multi-core supportLatest VxWorks7 RTOS support |
|------------------------|---|
| FPGA | Support high-speed input-output IOEW(electronic warfare) and Radar testing and verification equipment |
| Reliability Testing | Execute static test based on DAPA(Defense Acquisition Program Administration) standard Self-verification of reliability for RTNgine testing tool |





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